STACKED SEMICONDUCTOR MODULE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of, and claims priority to, prior U.S. Application No. 09/792,788, filed February 22, 2001, which application is U.S. Patent No. 6,720,643, incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates to semiconductor modules and in particular to multi-chip or stacked integrated circuit (IC) die modules having separately addressable IC dice.

BACKGROUND OF THE INVENTION

[0003] The semiconductor industry is constantly producing smaller and more complex semiconductors, sometimes called integrated circuits (ICs) or chips. This trend has brought about the need for smaller semiconductor packages with smaller footprints, higher lead counts, and better electrical and thermal performance, while at the same time meeting accepted reliability standards.

[0004] As memory demands increase, so does the need for increased memory capacity. A problem with adding more ICs to a circuit board for increased memory capacity, is that placement of the ICs on the circuit board is spread out, which often requires reconfiguration of the circuit board connectors and their associated connections on a motherboard. This ultimately leads to replacing the circuit board and in some cases the entire motherboard.

[0005] One solution to adding more memory capacity without spreading out ICs on a circuit board is by using a 3-dimensional chip stacking technique to form multi-chip modules (MCMs), otherwise known as stacked semiconductor modules, or stacked IC modules. These MCMs have a high memory capacity, while retaining a relatively small size. Examples of these techniques are disclosed in United States Patent numbers 5,104,820, and 5,279,991, and United States Patent Application